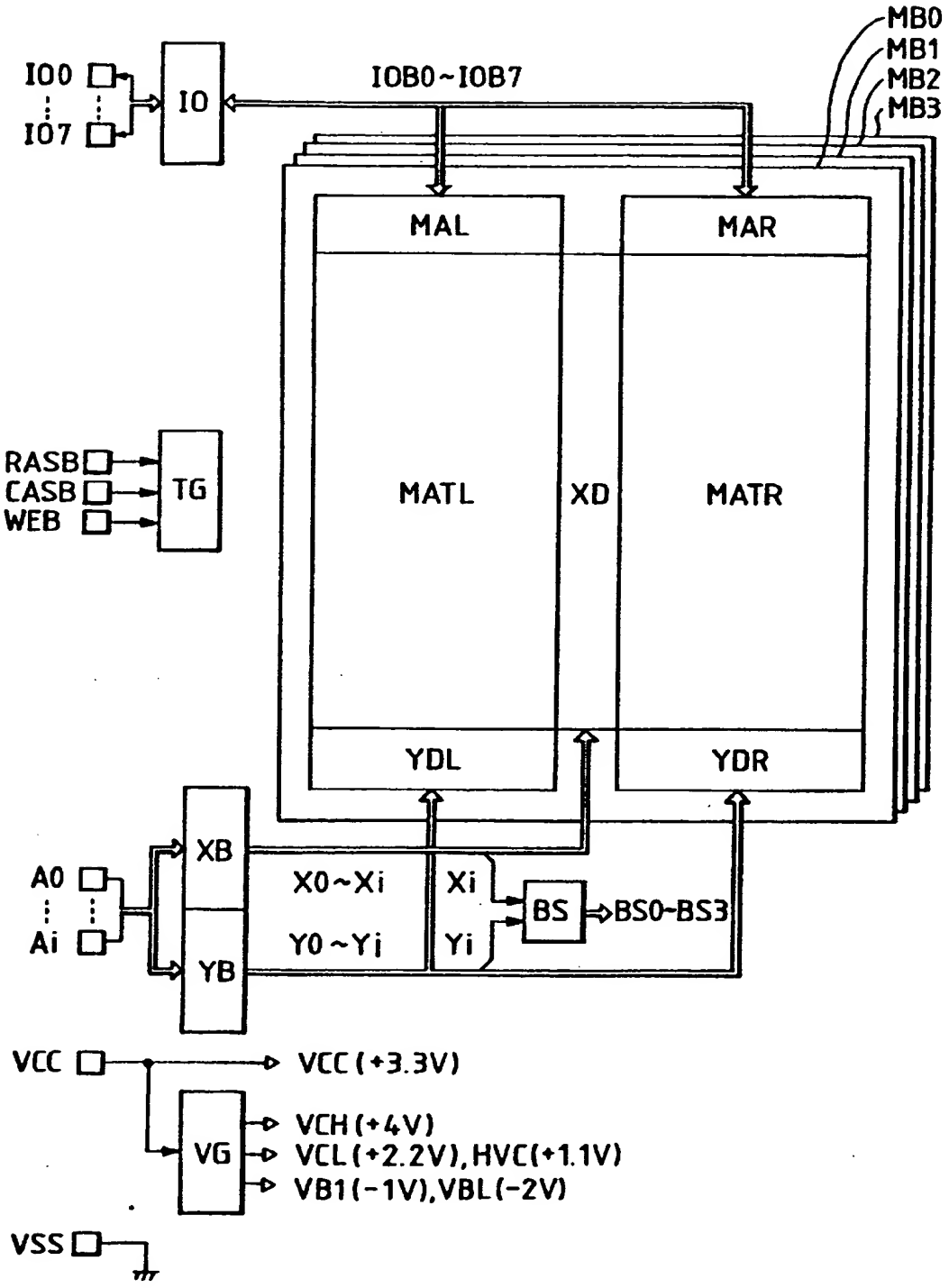
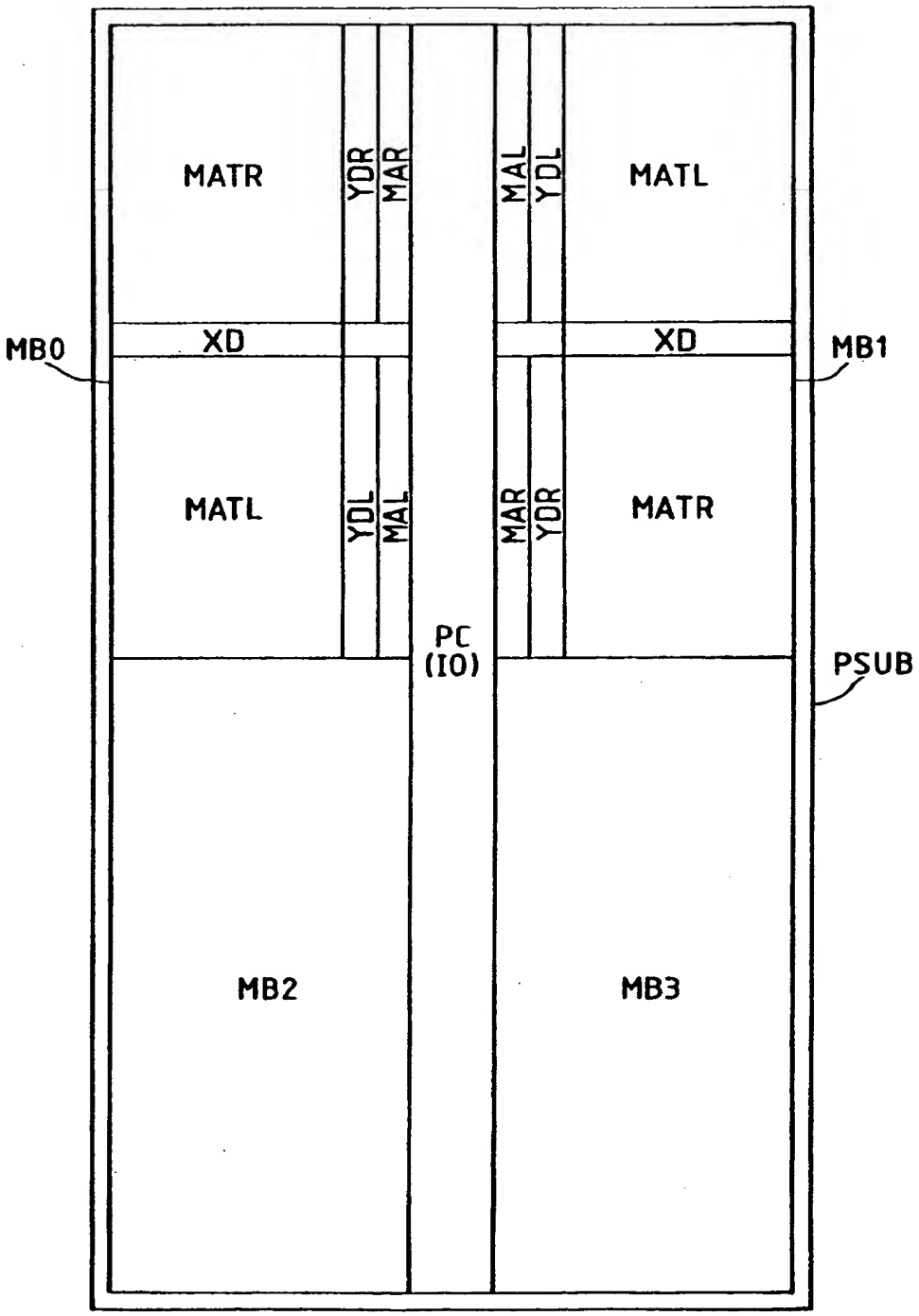
FIG. 1



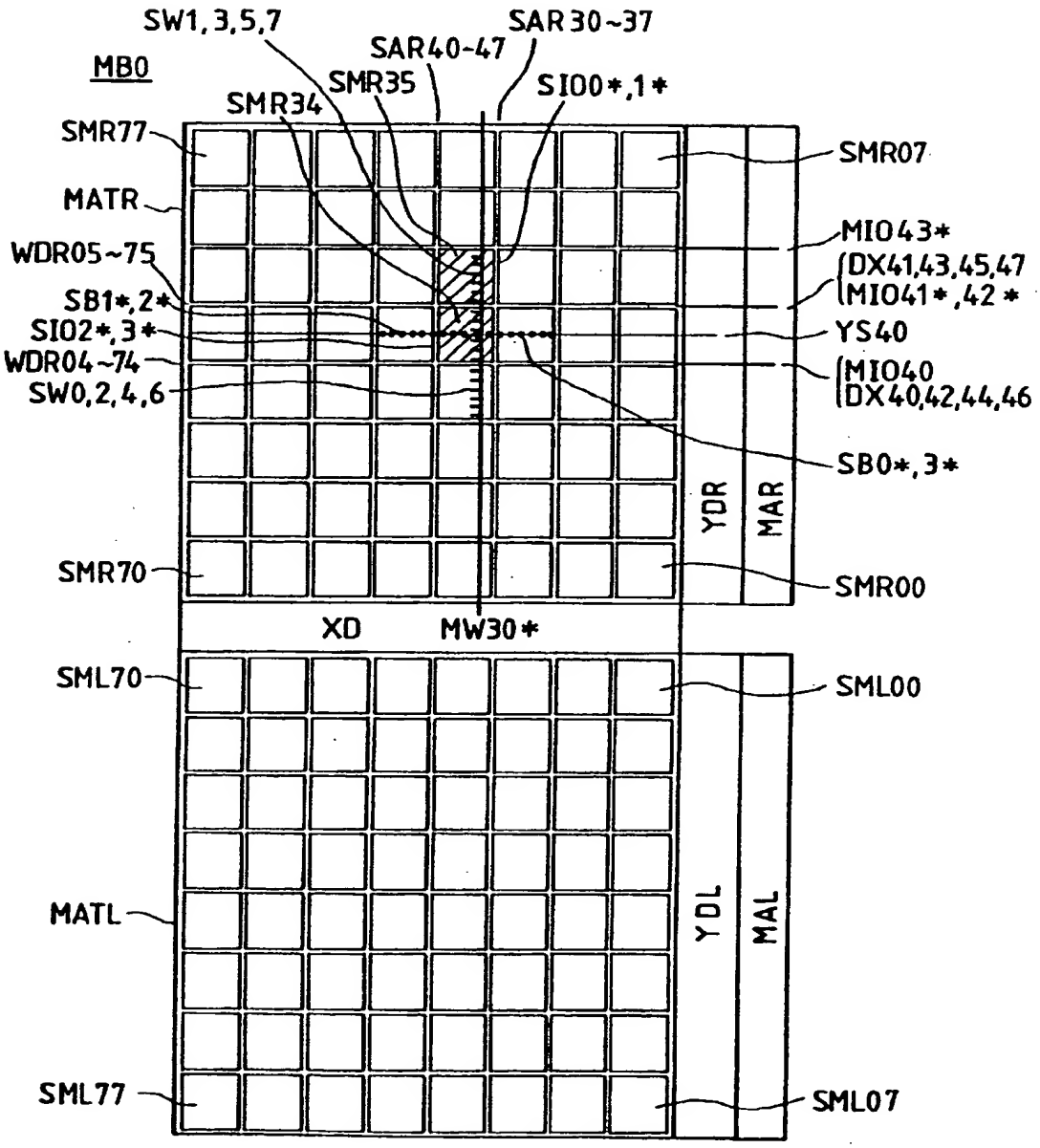
Patent: 5,966,341

FIG. 2



Patent-5966341

FIG. 3



Doc No. 5966341

FIG. 4

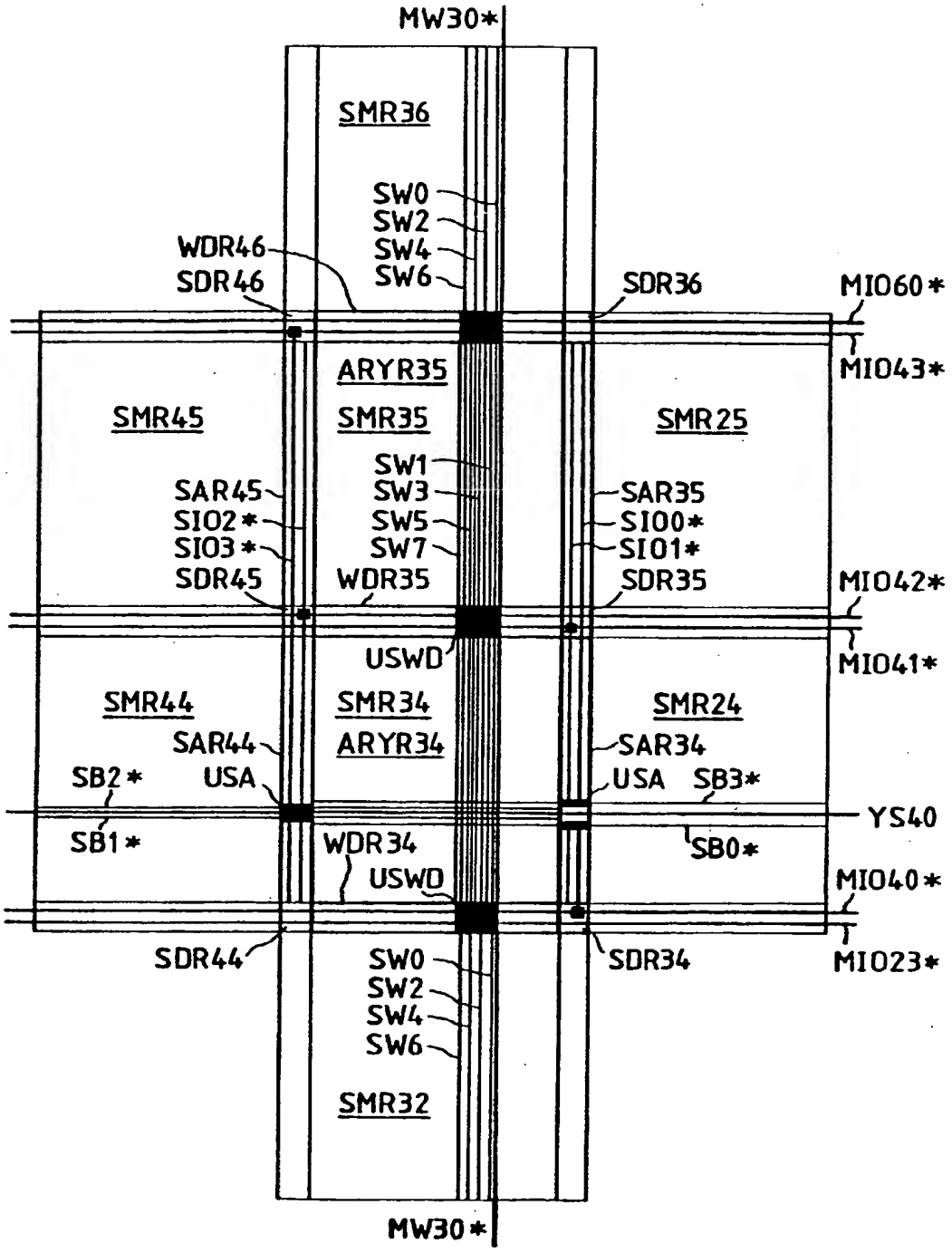

MW30*
SMR36
SW0
SW2
SW4
SW6
WDR46
SDR46
SDR36
MIO60*
MIO43*
ARYR35
SMR45
SMR35
SMR25
SW1
SW3
SW5
SW7
SAR45
SIO2*
SIO3*
SDR45
WDR35
SAR35
SIO0*
SIO1*
SDR35
MIO42*
MIO41*
USWD
SMR44
SMR34
SMR24
SAR44
ARYR34
SAR34
SB2*
USA
USA
SB3*
YS40
SB1*
WDR34
USWD
SB0*
MIO40*
SDR44
SDR34
MIO23*
SW0
SW2
SW4
SW6
SMR32
MW30*

FIG. 5

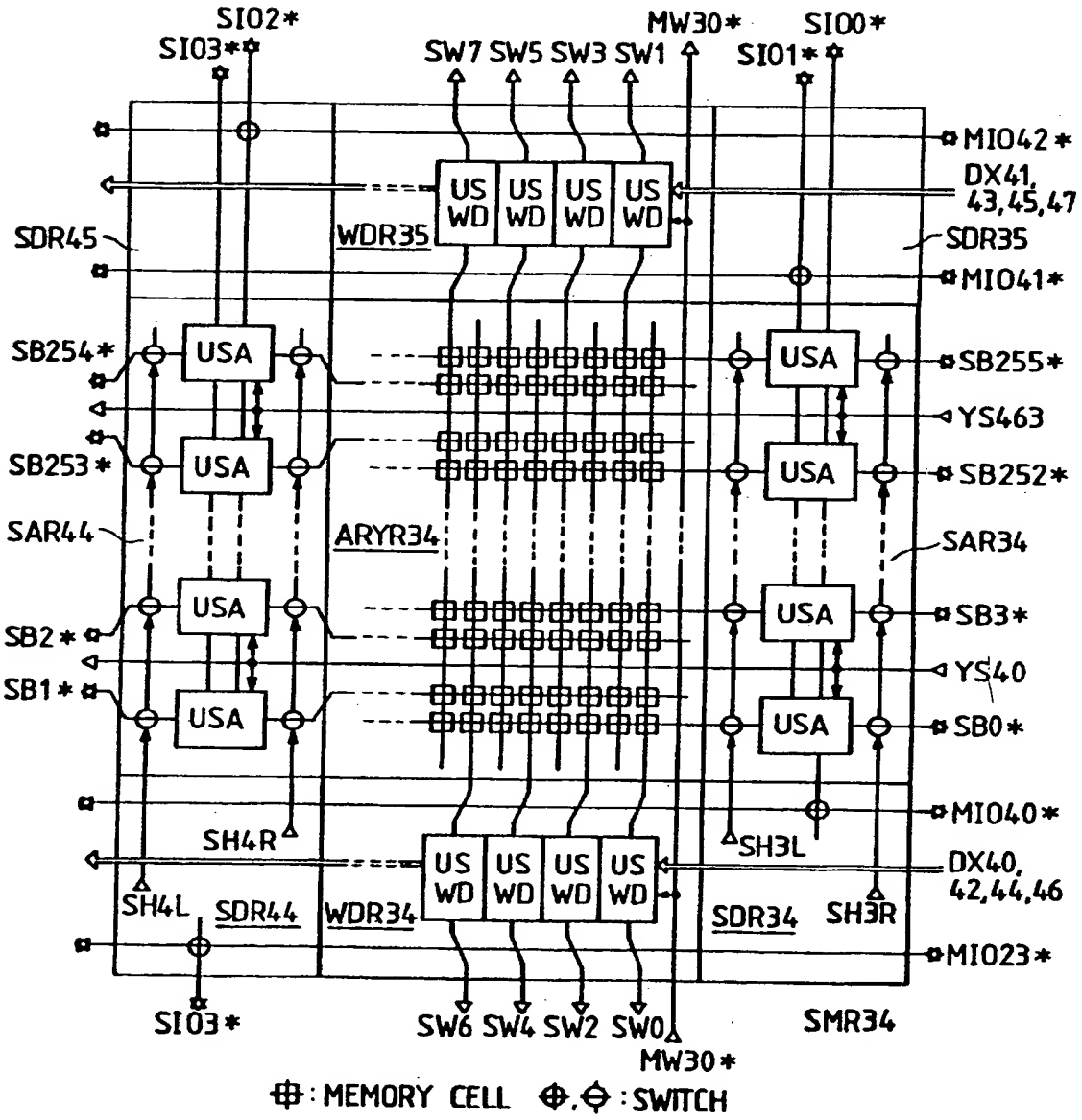

SI02*
SI03*
MW30*
SI00*
SW7 SW5 SW3 SW1
SI01*
MIO42*
DX41, 43,45,47
US WD
WDR35
SDR45
SDR35
MIO41*
SB254*
USA
SB255*
YS463
SB253*
SB252*
SAR44
ARYR34
SAR34
SB2*
SB3*
YS40
SB1*
SB0*
MIO40*
SH4R
SH3L
DX40, 42,44,46
SH4L
SDR44
WDR34
SDR34
SH3R
MIO23*
SI03*
SW6 SW4 SW2 SW0
SMR34
MW30*
: MEMORY CELL
: SWITCH

FIG. 6

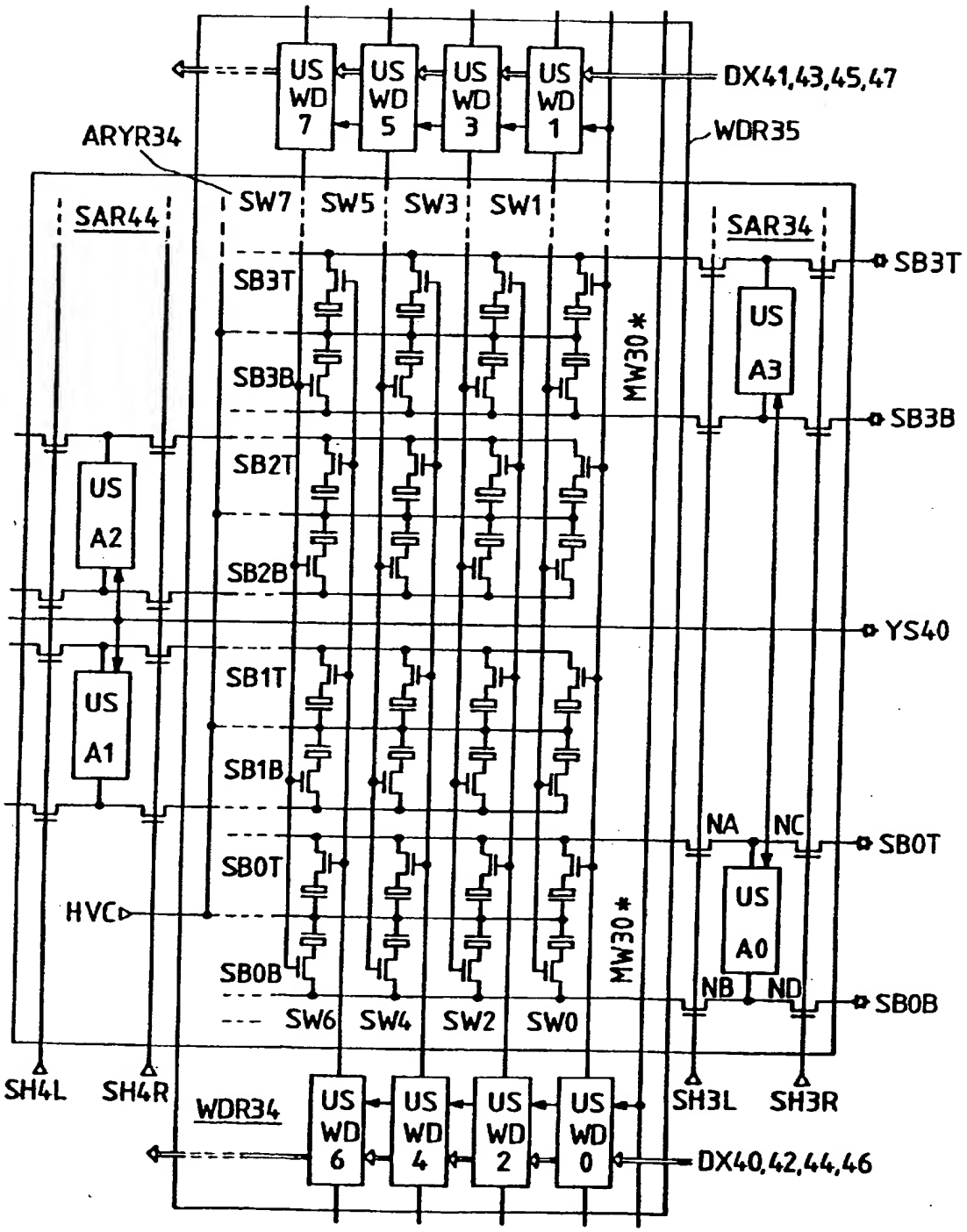

USWD7
USWD5
USWD3
USWD1
DX41,43,45,47
WDR35
ARYR34
SAR44
SAR34
SW7
SW5
SW3
SW1
SB3T
SB3B
SB2T
SB2B
SB1T
SB1B
SB0T
SB0B
MW30*
USA3
USA2
USA1
USA0
YS40
NA
NC
NB
ND
HVC
SW6
SW4
SW2
SW0
SH4L
SH4R
WDR34
USWD6
USWD4
USWD2
USWD0
DX40,42,44,46
SH3L
SH3R

FIG. 7(A)

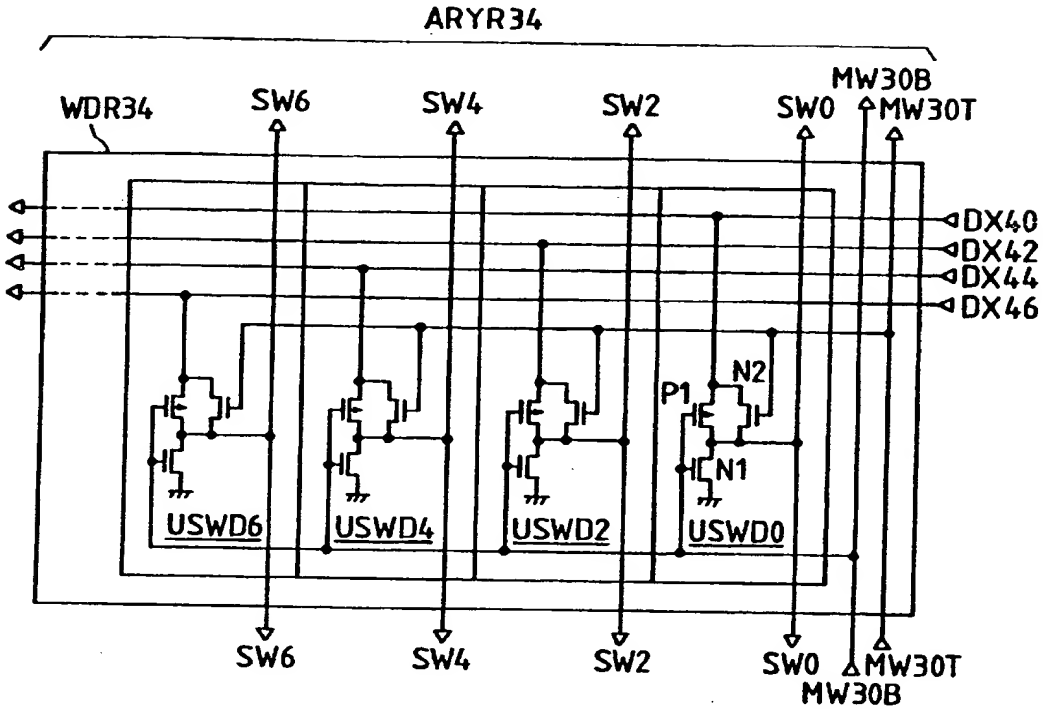
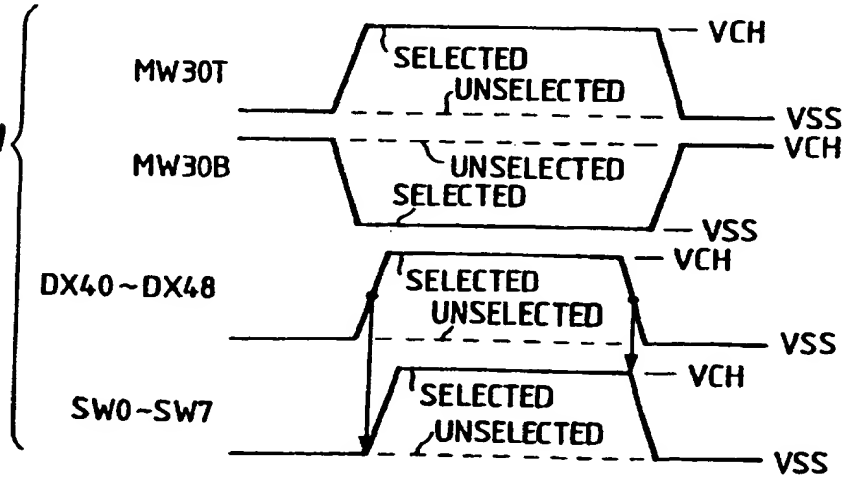


FIG. 7(B)



Patent-5,966,341

FIG. 8(A)

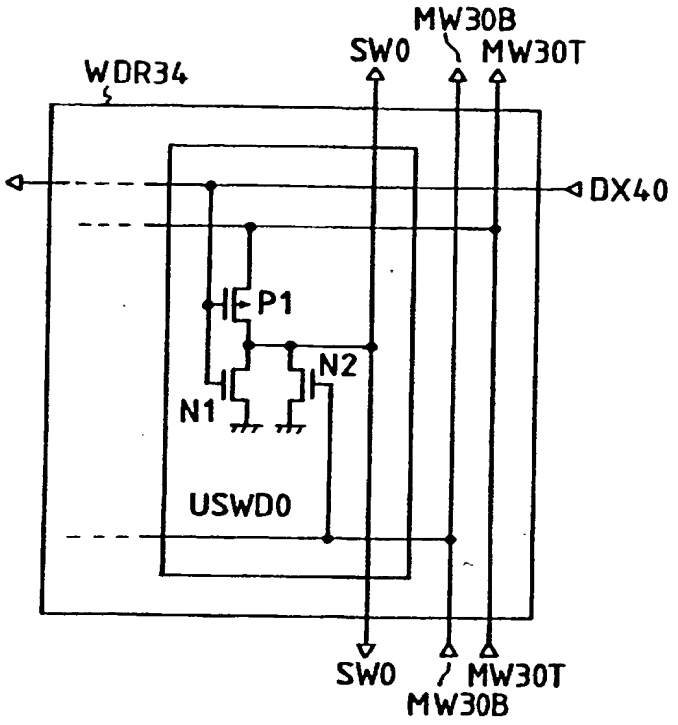

MW30B
SW0
MW30T
WDR34
DX40
P1
N2
N1
USWD0
SW0
MW30T
MW30B

FIG. 8(B)

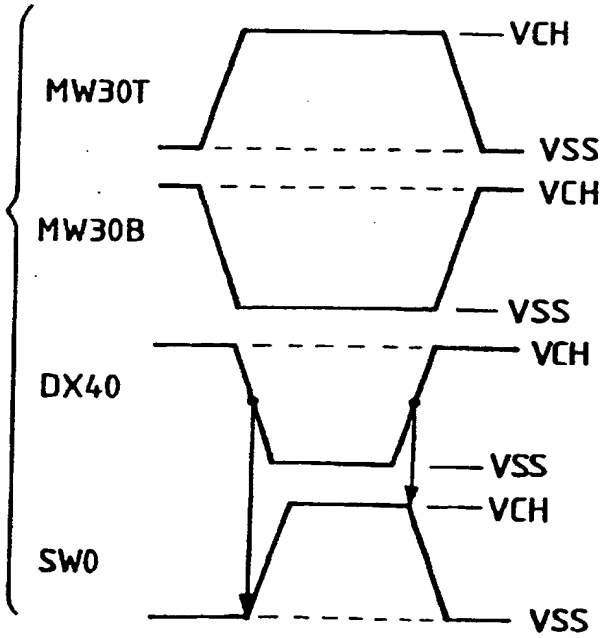

MW30T
VCH
VSS
MW30B
VCH
VSS
DX40
VCH
VSS
VCH
SW0
VSS

FIG. 9(A)

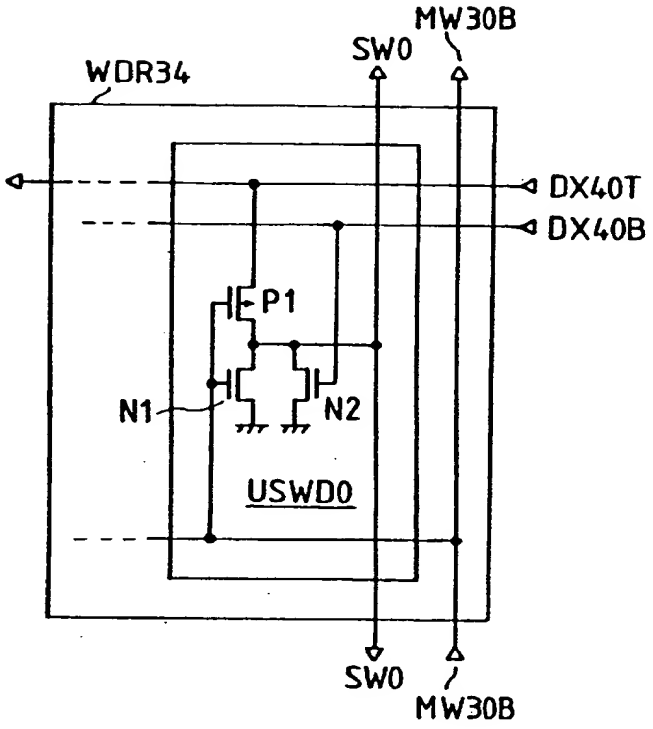
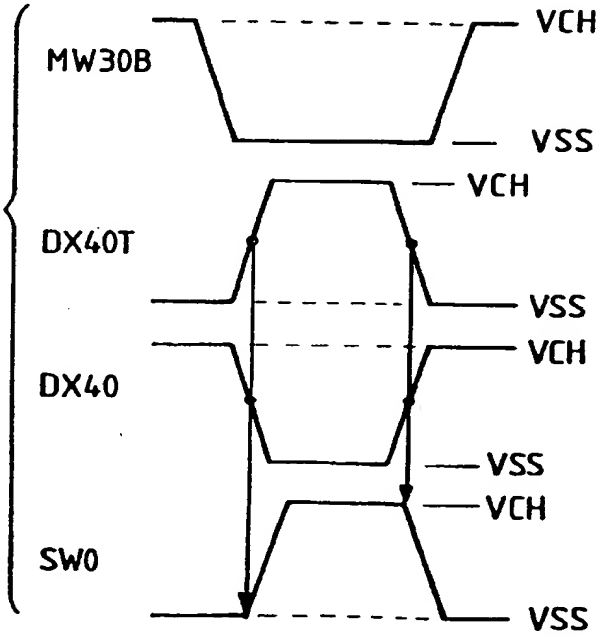
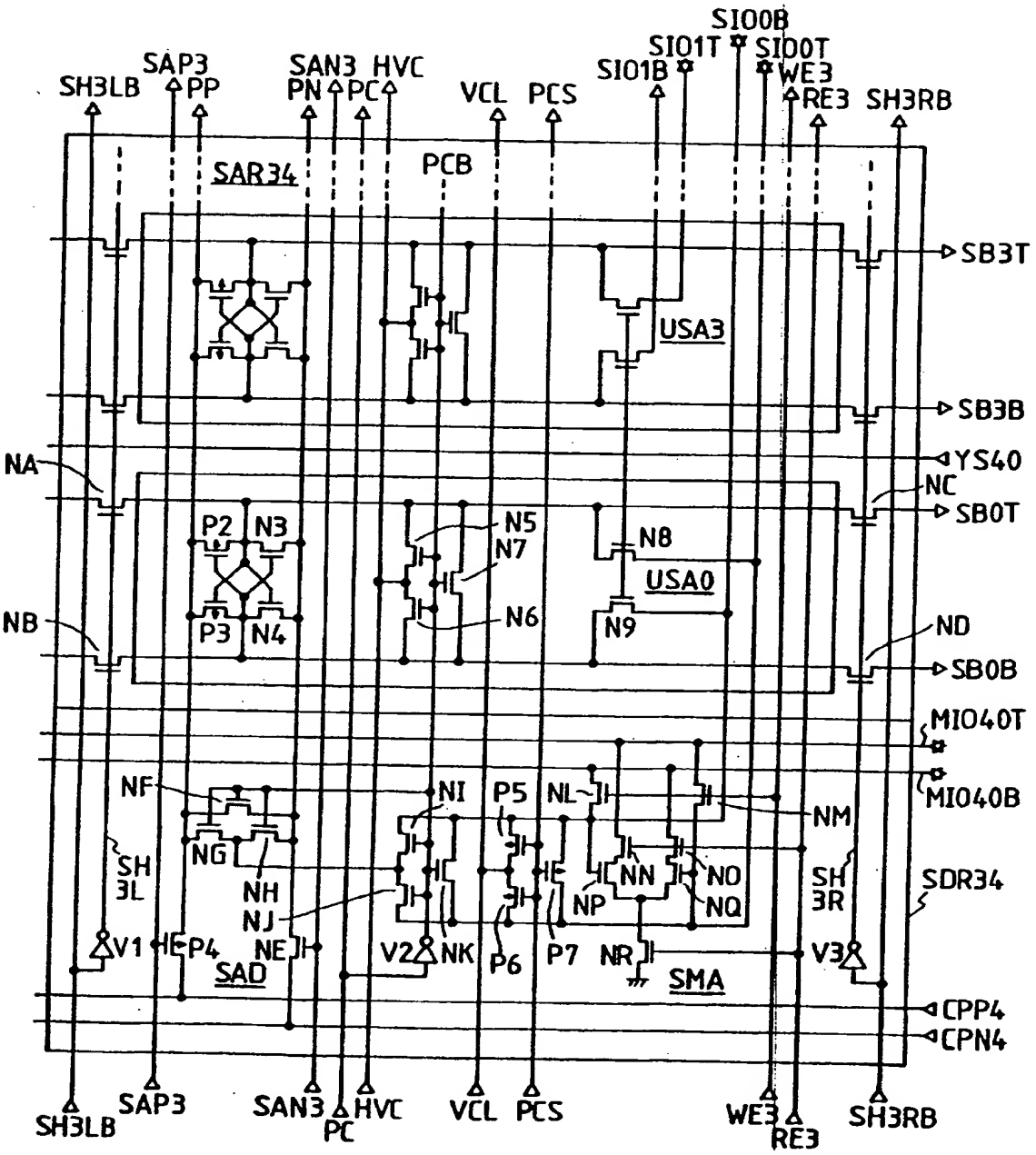


FIG. 9(B)



FOREIGN PATENT 2964560

FIG. 10


SI00B
SI01T
SI00T
SAP3
SAN3
HVC
SI01B
WE3
SH3LB
PP
PN
PC
VCL
PCS
RE3
SH3RB
SAR34
PCB
SB3T
USA3
SB3B
NA
YS40
NC
SB0T
P2
N3
N5
N7
N8
USA0
NB
P3
N4
N6
N9
ND
SB0B
MI040T
MI040B
NF
NI
P5
NL
NM
SH
3L
NG
NH
NJ
NN
NO
NQ
NP
SH
3R
SDR34
V1
P4
NE
V2
NK
P6
P7
NR
V3
SAD
SMA
CPP4
CPN4
SH3LB
SAP3
SAN3
HVC
PC
VCL
PCS
WE3
RE3
SH3RB

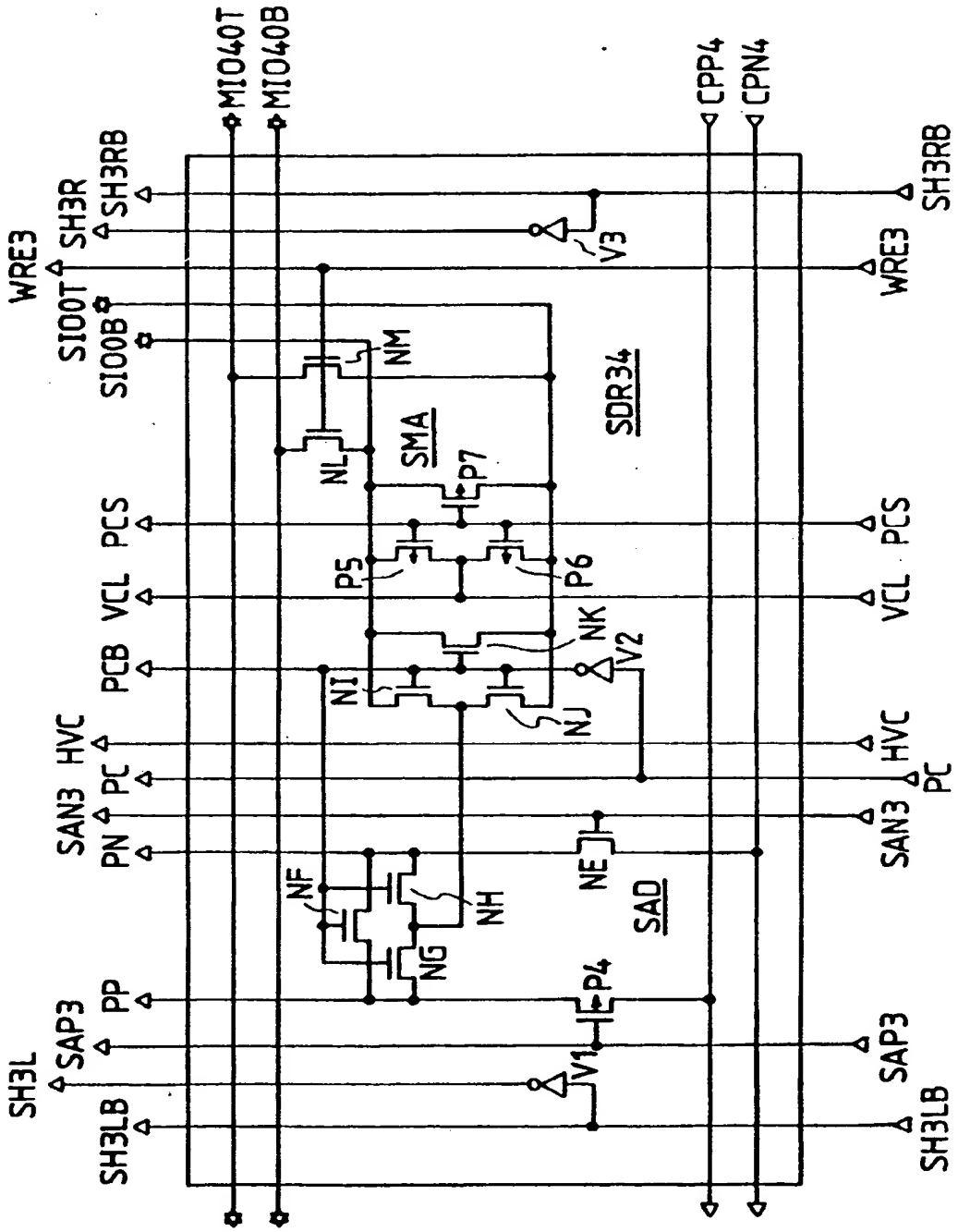

MIO40T
MIO40B
CPP4
CPN4
SH3RB
SH3R
V3
WRE3
SIOOT
SIOOB
NM
SDR34
SMA
NL
P7
PCS
P5
P6
VCL
NK
PCB
V2
NI
NJ
HVC
SAN3
PC
PN
NE
NF
NH
SAD
NG
P4
PP
SAP3
V1
SH3L
SH3LB

FIG. 11

FIG. 12

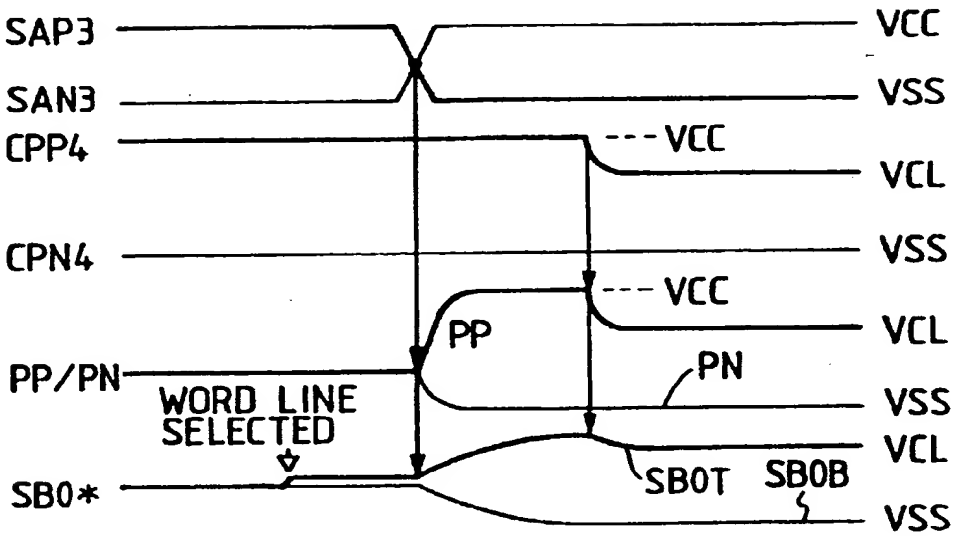
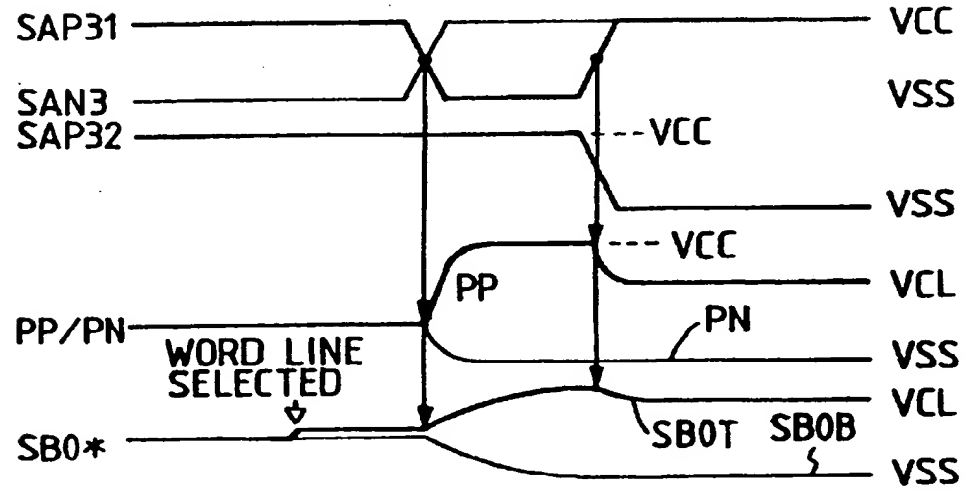

SAP3
SAN3
CPP4
CPN4
PP/PN
SB0*
WORD LINE SELECTED
PP
PN
SB0T
SB0B
VCC
VSS
VCL

FIG. 14


SAP31
SAN3
SAP32
PP/PN
SB0*
WORD LINE SELECTED
PP
PN
SB0T
SB0B
VCC
VSS
VCL

Patent 5,966,341

FIG. 13

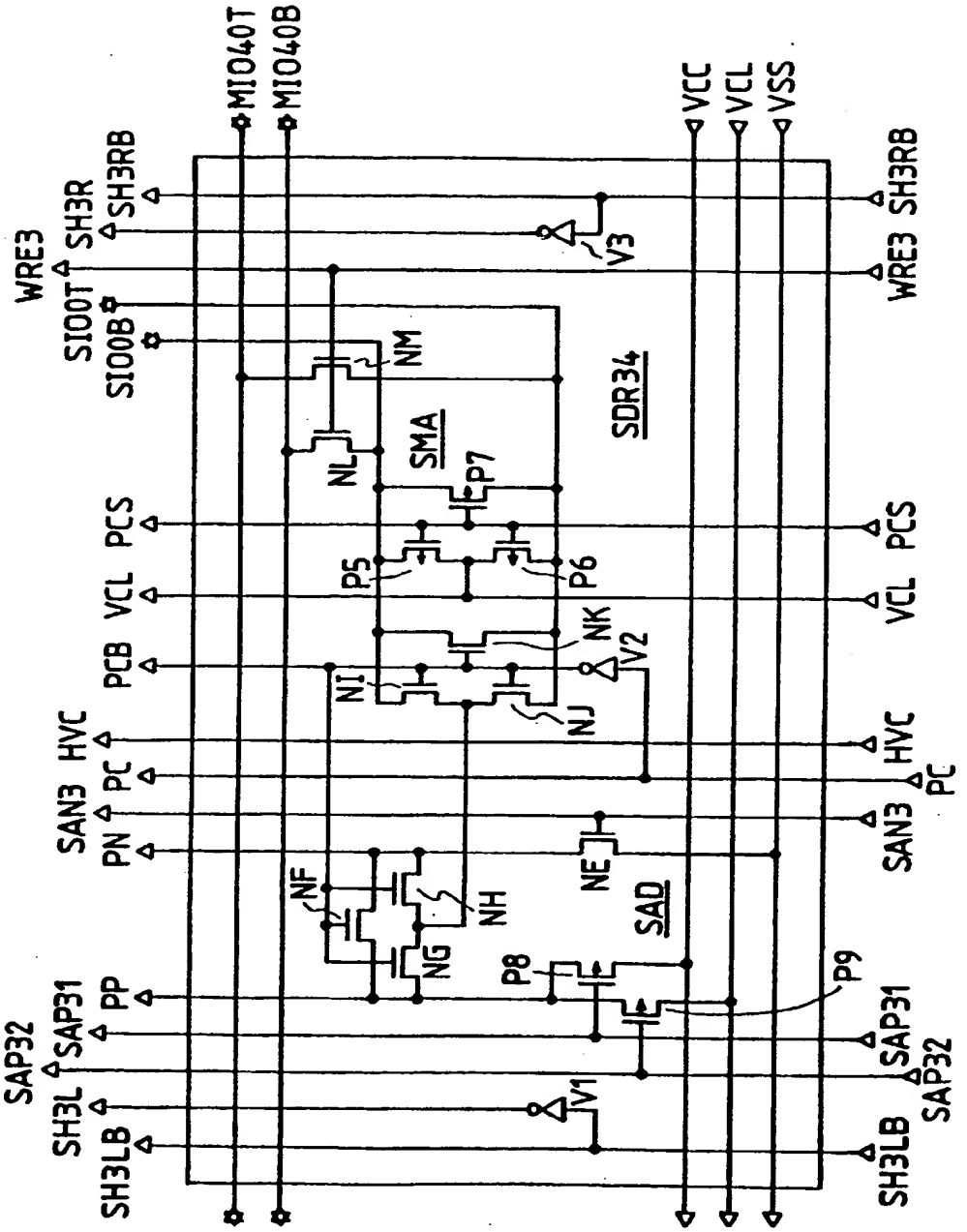
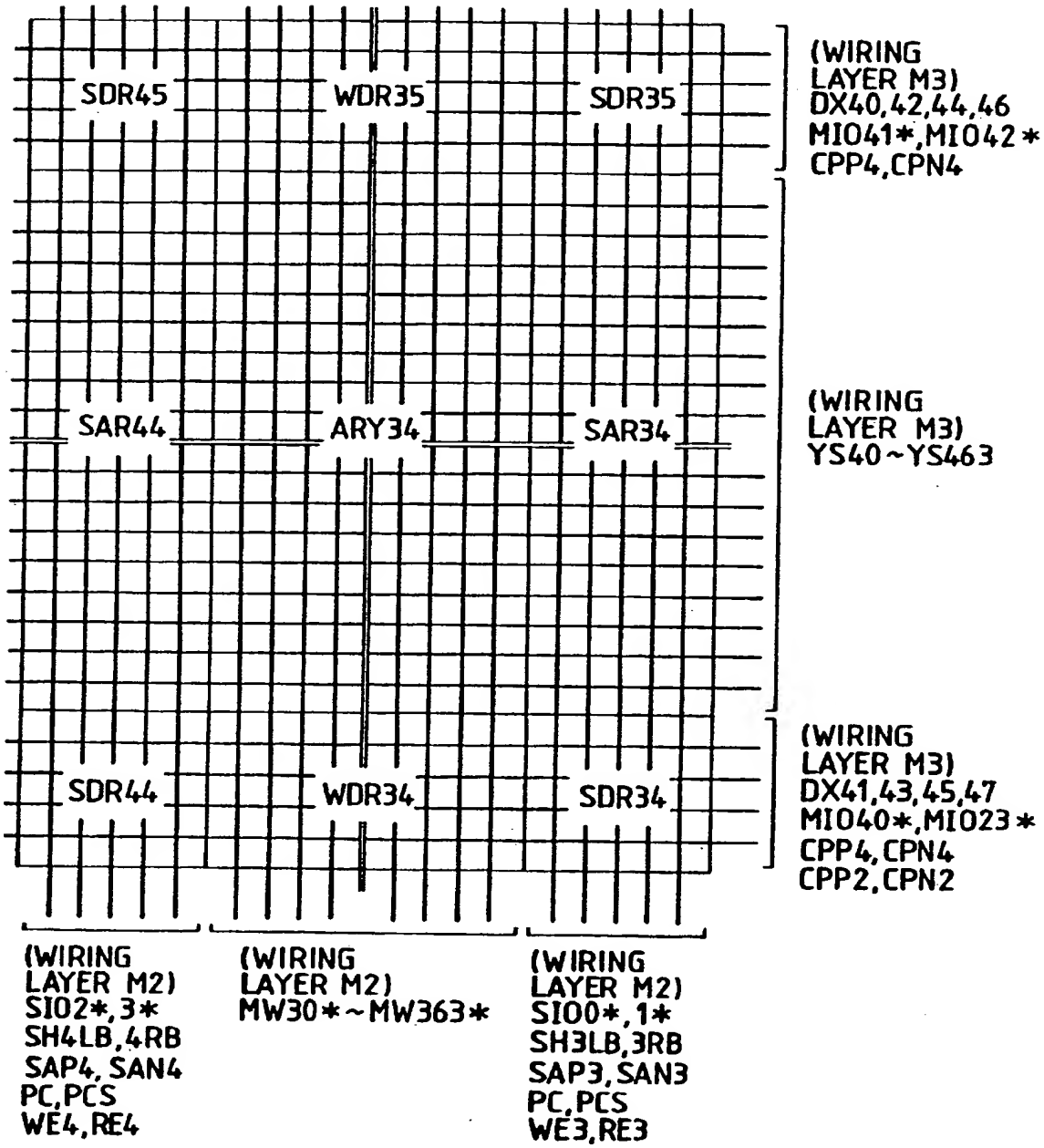
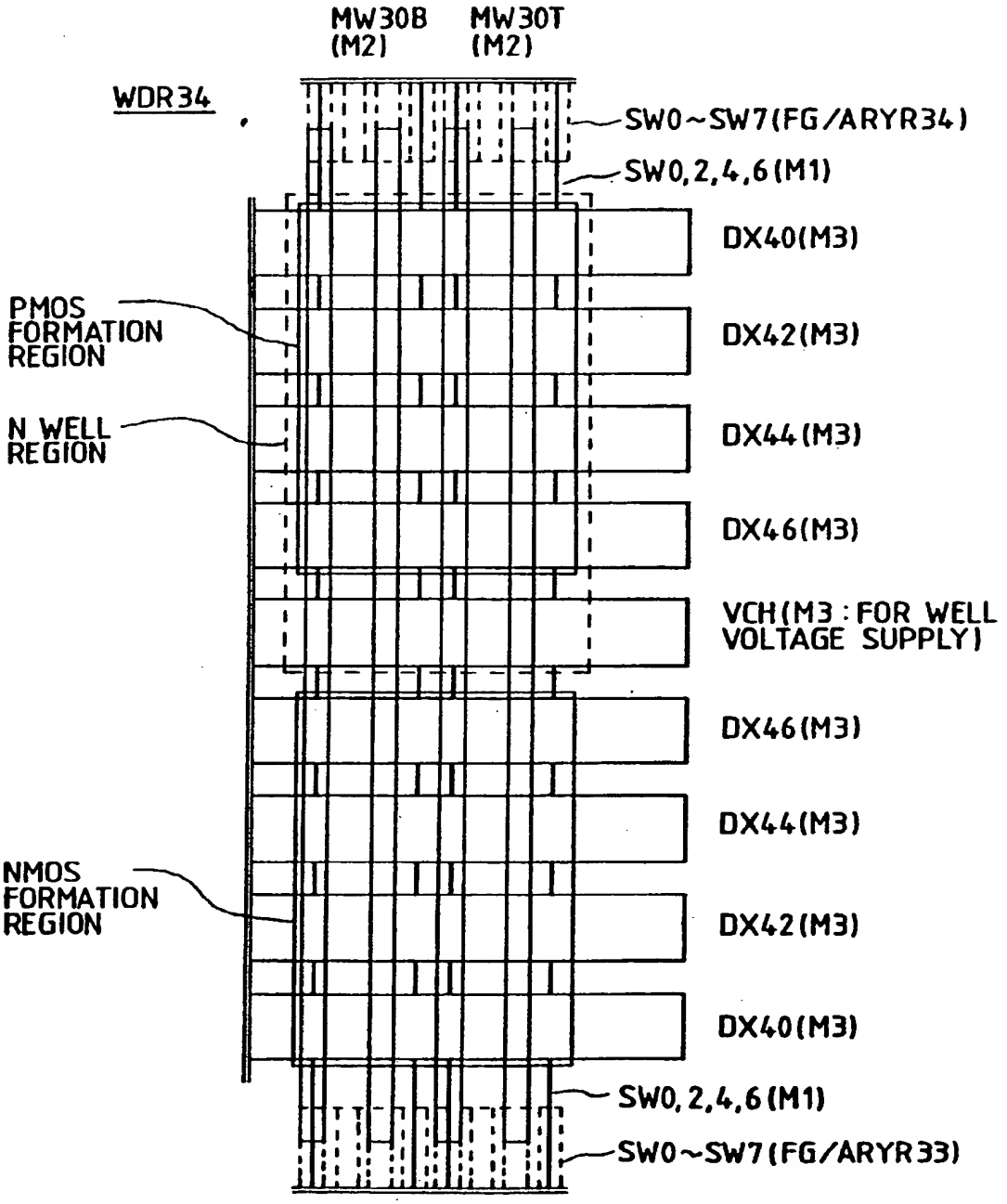


FIG. 15



Patent-5,966,360

FIG. 16



TOSHIBA 5964560

FIG. 17

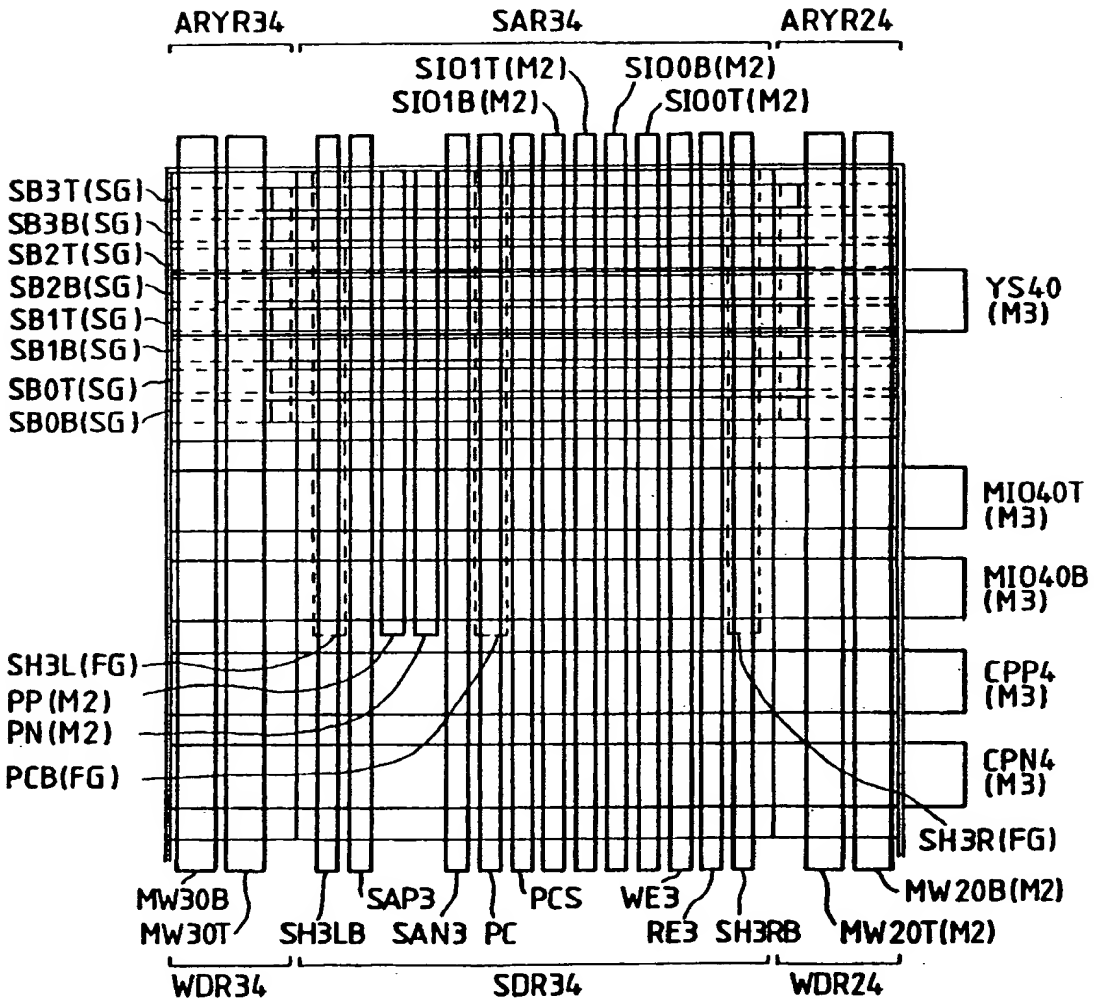
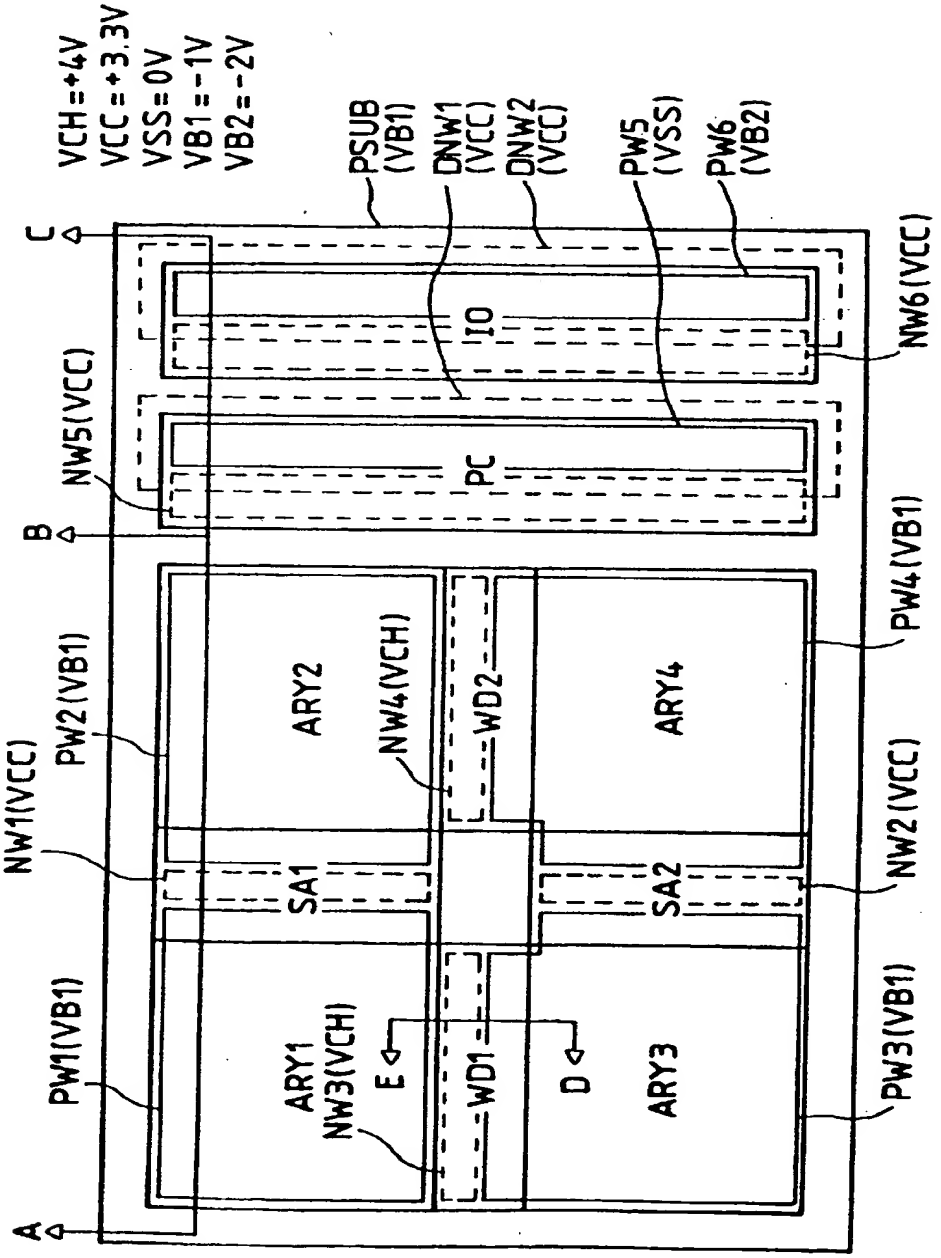

ARYR34
SAR34
ARYR24
SIO1T(M2)
SIO0B(M2)
SIO1B(M2)
SIO0T(M2)
SB3T(SG)
SB3B(SG)
SB2T(SG)
SB2B(SG)
SB1T(SG)
SB1B(SG)
SB0T(SG)
SB0B(SG)
YS40 (M3)
MIO40T (M3)
MIO40B (M3)
CPP4 (M3)
CPN4 (M3)
SH3L(FG)
PP(M2)
PN(M2)
PCB(FG)
SH3R(FG)
MW30B
MW30T
SH3LB
SAP3
SAN3
PC
PCS
WE3
RE3
SH3RB
MW20B(M2)
MW20T(M2)
WDR34
SDR34
WDR24

FIG. 18


VCH=+4V
VCC=+3.3V
VSS=0V
VB1=-1V
VB2=-2V
PSUB (VB1)
DNW1 (VCC)
DNW2 (VCC)
PW5 (VSS)
PW6 (VB2)
C
B
A
NW6(VCC)
NW5(VCC)
IO
PC
PW4(VB1)
PW2(VB1)
NW1(VCC)
ARY2
NW4(VCH)
WD2
ARY4
SA1
SA2
NW2(VCC)
PW1(VB1)
ARY1
NW3(VCH)
E
WD1
D
ARY3
PW3(VB1)

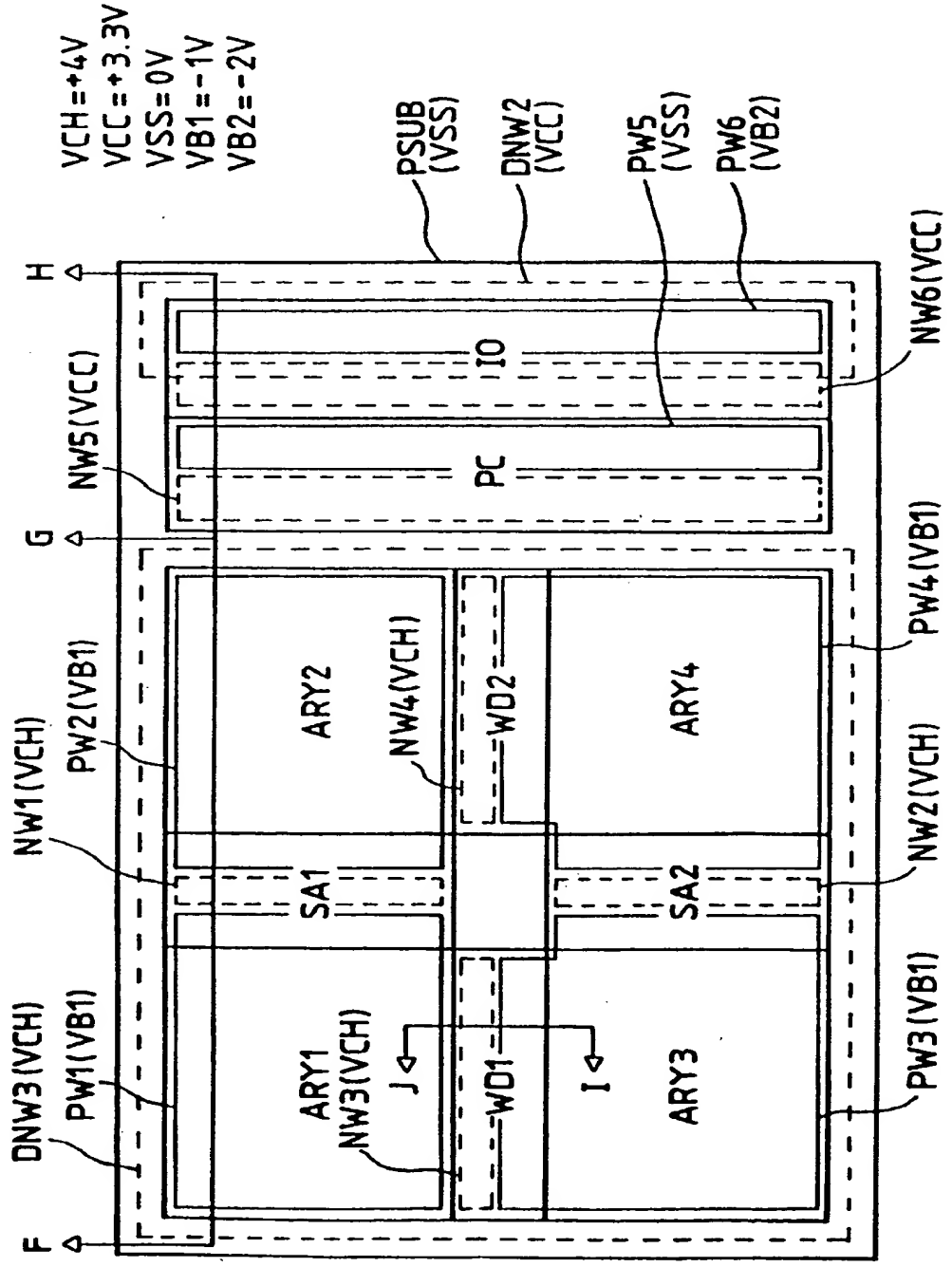

VCH=+4V
VCC=+3.3V
VSS=0V
VB1=-1V
VB2=-2V
PSUB (VSS)
DNW2 (VCC)
PW5 (VSS)
PW6 (VB2)
NW6(VCC)
NW5(VCC)
IO
PC
ARY2
NW4(VCH)
WD2
ARY4
PW4(VB1)
NW1(VCH)
PW2(VB1)
SA1
SA2
NW2(VCH)
ARY1
NW3(VCH)
WD1
ARY3
PW3(VB1)
DNW3(VCH)
PW1(VB1)
H
G
F
J
I

FIG. 19

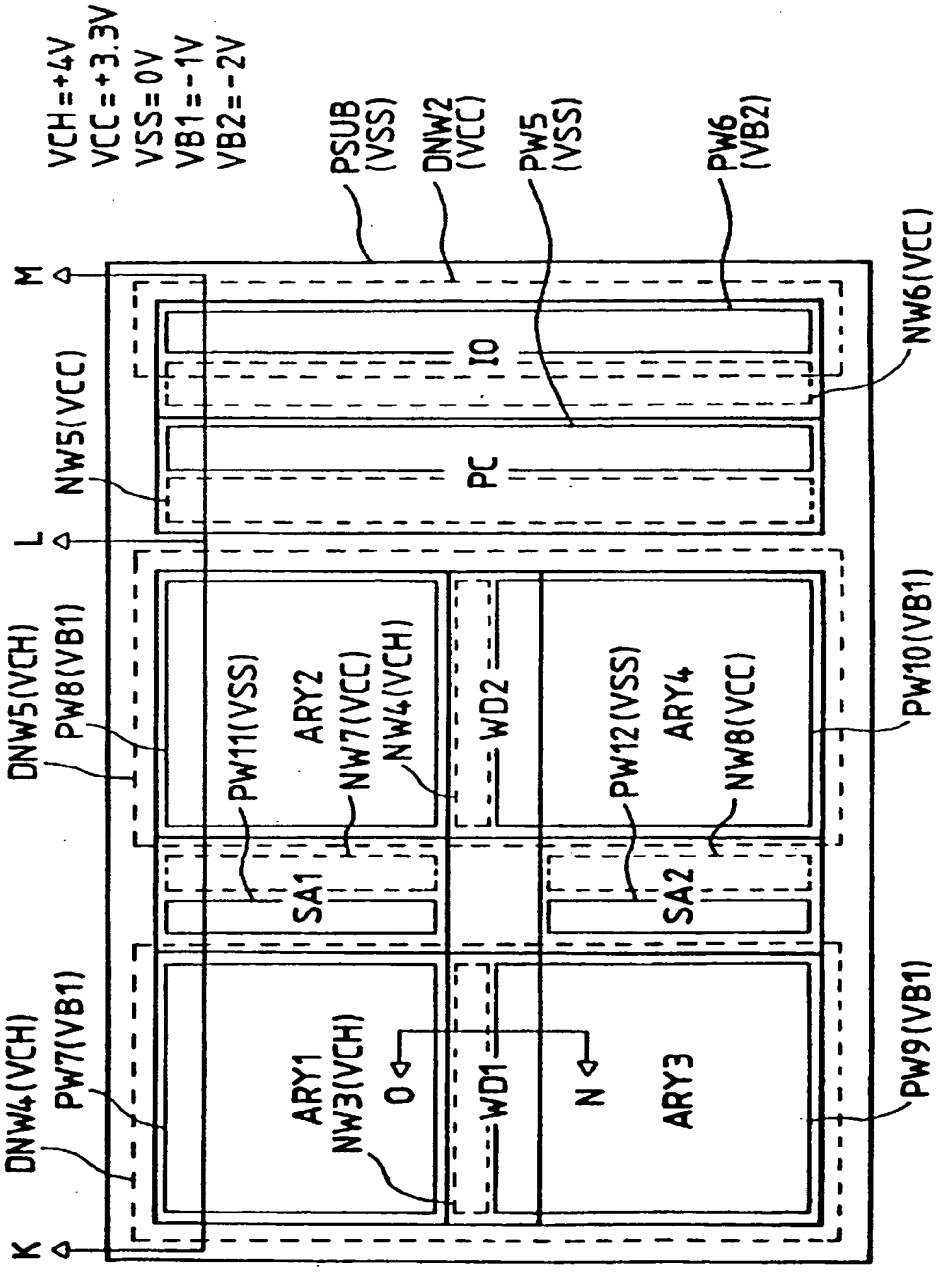

VCH=+4V
VCC=+3.3V
VSS=0V
VB1=-1V
VB2=-2V
PSUB (VSS)
DNW2 (VCC)
PW5 (VSS)
PW6 (VB2)
M
L
K
NW5(VCC)
NW6(VCC)
IO
PC
DNW5(VCH)
PW8(VB1)
PW11(VSS)
ARY2
NW7(VCH)
NW4(VCH)
WD2
PW12(VSS)
ARY4
NW8(VCC)
PW10(VB1)
SA1
SA2
DNW4(VCH)
PW7(VB1)
ARY1
NW3(VCH)
O
WD1
N
ARY3
PW9(VB1)

FIG. 20

FIG. 21(A)

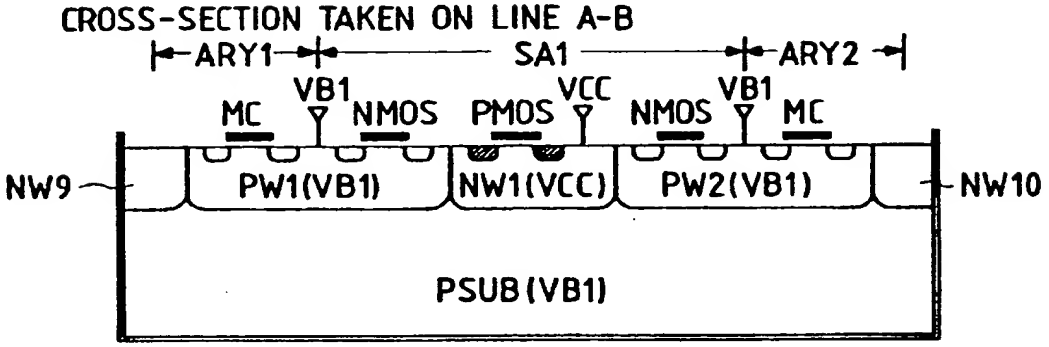


FIG. 21(B)

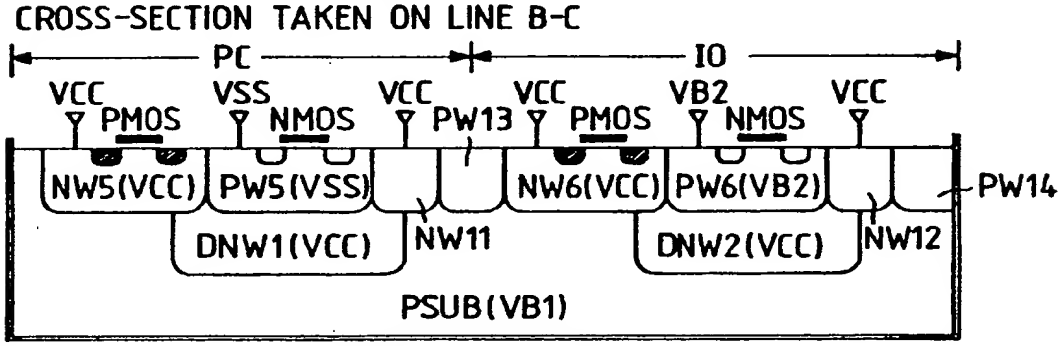
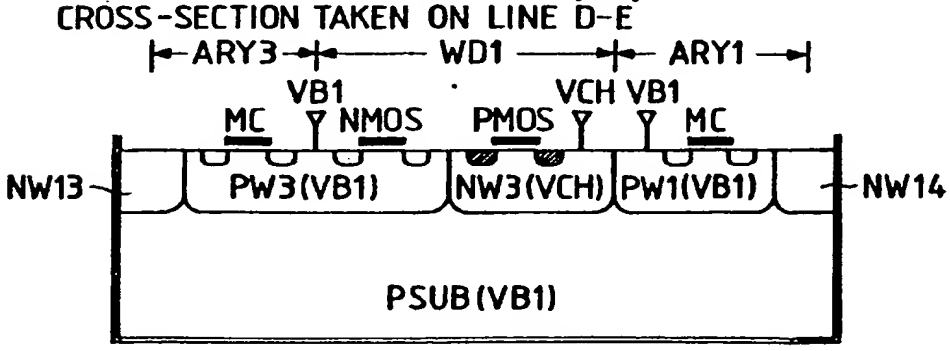


FIG. 21(C)



: P+ DIFFUSION LAYER : N+ DIFFUSION LAYER

VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

FIG. 22(A)

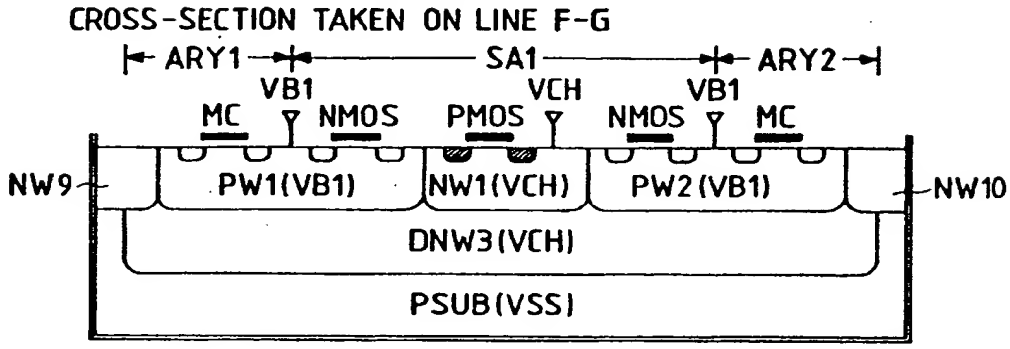


FIG. 22(B)

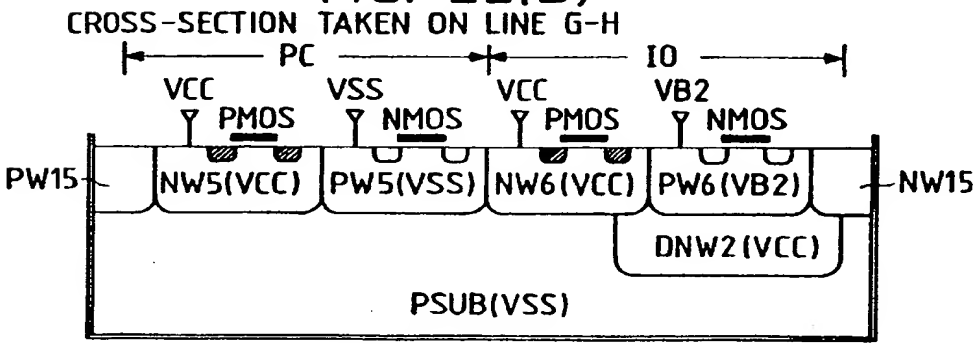
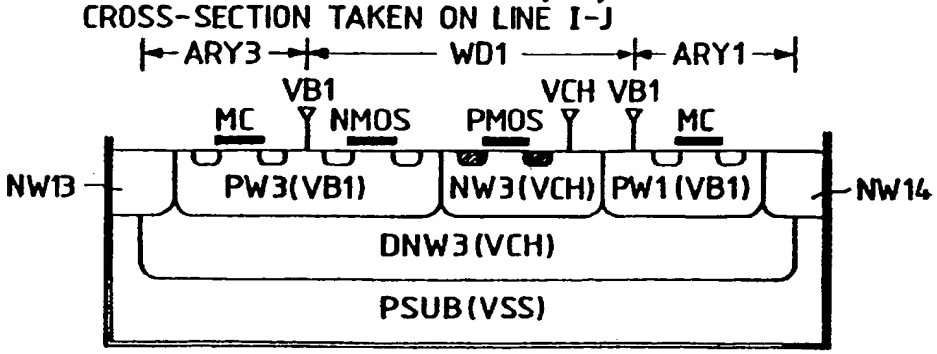


FIG. 22(C)



: P^+ DIFFUSION LAYER : N^+ DIFFUSION LAYER

VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

Patent: 5,966,341

FIG. 23(A)

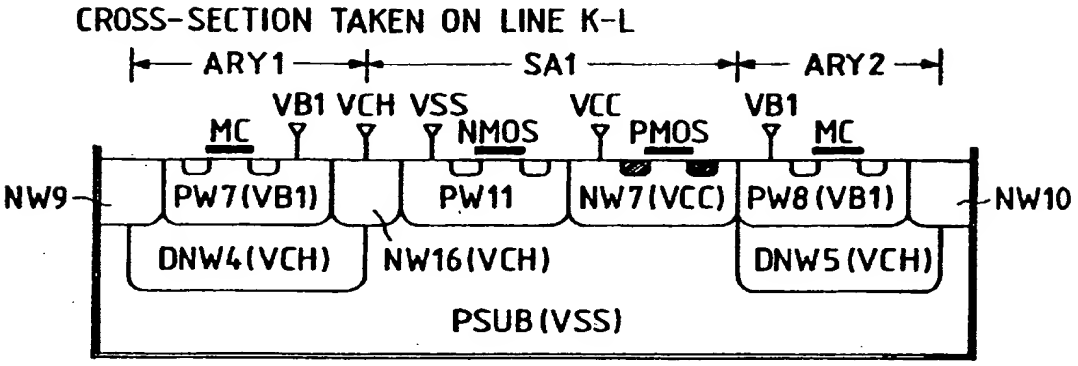


FIG. 23(B)

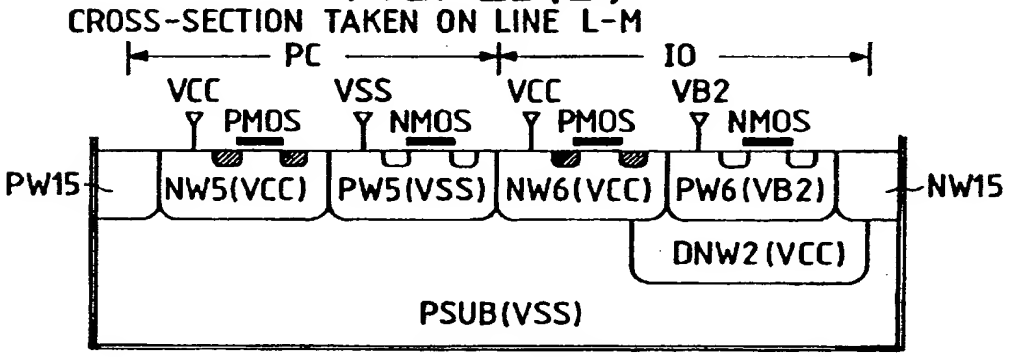
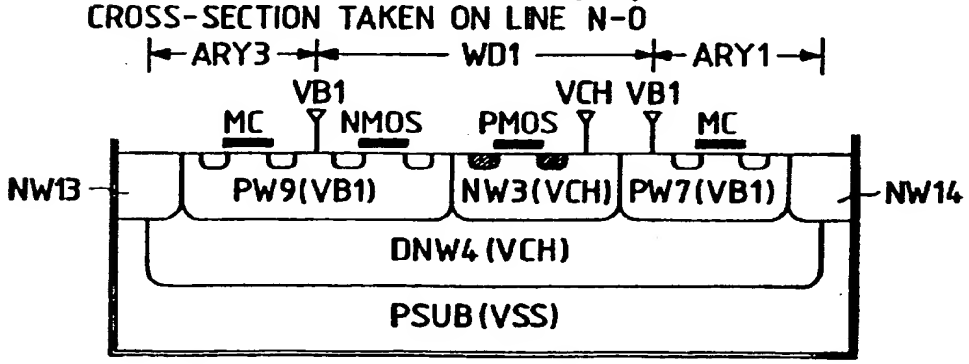


FIG. 23(C)



: P^+ DIFFUSION LAYER : N^+ DIFFUSION LAYER

VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V